Complementary MOSFET Half-Bridge (N- and P-Channel)

CHARACTERISTICS

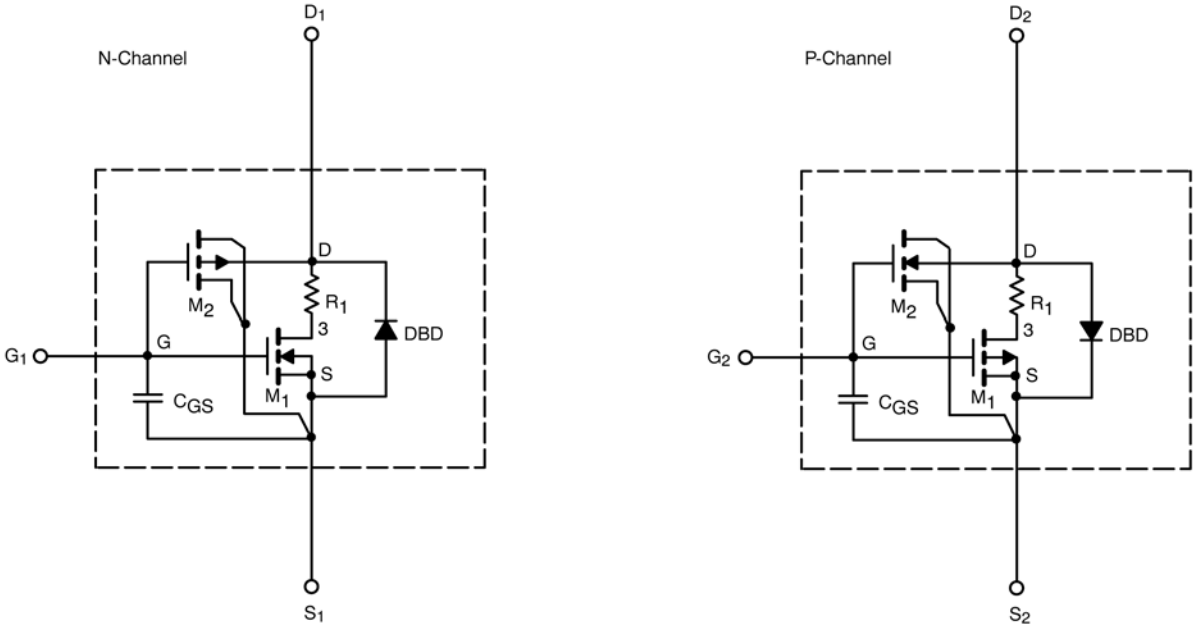
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



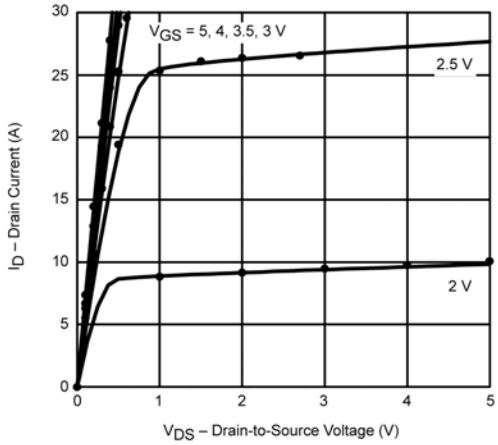
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

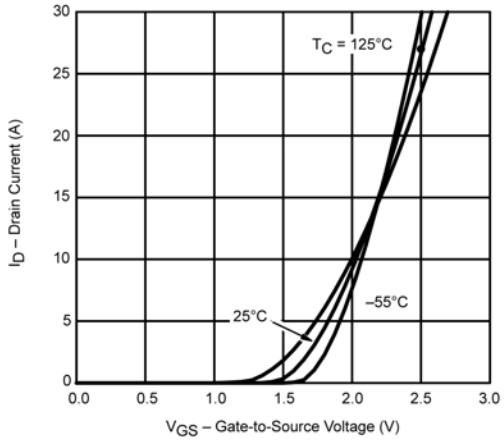
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	0.96		
		V_{DS} = V_{GS}, I_D = –250 μA	P-Ch	0.91		
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N-Ch	394		A
		V_{DS} = –5 V, V_{GS} = –4.5 V	P-Ch	63		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 9.1 A	N-Ch	0.015	0.016	Ω
		V_{GS} = –4.5 V, I_D = –5.3 A	P-Ch	0.047	0.048	
		V_{GS} = 2.5 V, I_D = 7.5 A	N-Ch	0.022	0.024	
		V_{GS} = –2.5 V, I_D = –4.1 A	P-Ch	0.102	0.082	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 9.1 A	N-Ch	26	29	S
		V_{DS} = –15 V, I_D = –5.3 A	P-Ch	10	11	
Diode Forward Voltage[a]	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V	N-Ch	0.80	0.80	V
		I_S = –2.1 A, V_{GS} = 0 V	P-Ch	0.80	–0.80	
Dynamic[b]						
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 9.1 A P-Channel V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –5.3 A	N-Ch	10	11	nC
			P-Ch	5	6	
Gate-Source Charge	Q_{gs}		N-Ch	2.5	2.5	
			P-Ch	1.3	1.3	
Gate-Source Charge	Q_{gs}		N-Ch	3.2	3.2	
			P-Ch	1.6	1.6	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = – 10 V, R_L = 10 Ω $I_D \cong$ –1 A, V_{GEN} = – 4.5 V, R_G = 6 Ω	N-Ch	50	35	ns
			P-Ch	14	20	
Rise Time	t_r		N-Ch	32	50	
			P-Ch	29	35	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	24	31	
			P-Ch	37	55	
Fall Time	t_f		N-Ch	14	15	
			P-Ch	56	35	

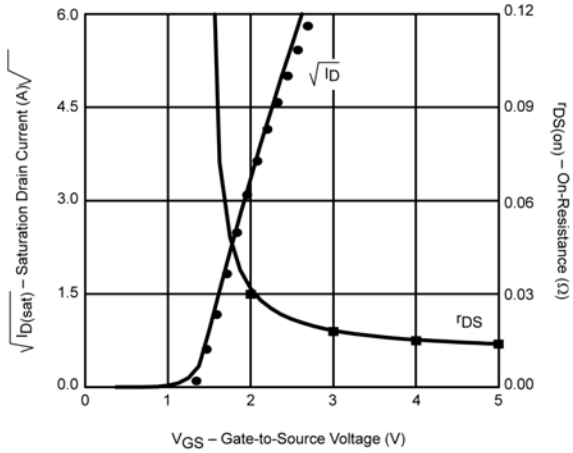
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

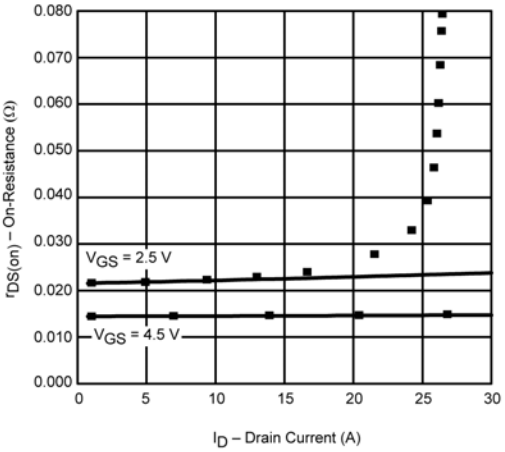
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

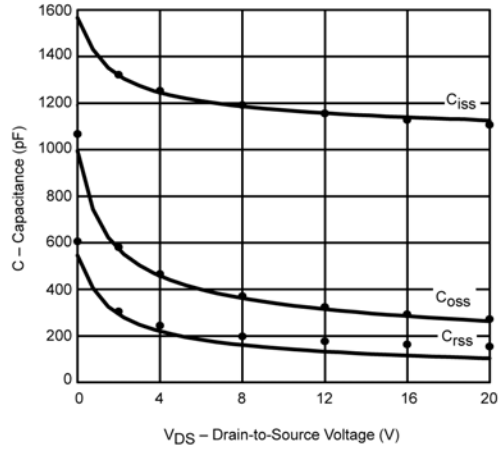
N-Channel MOSFET

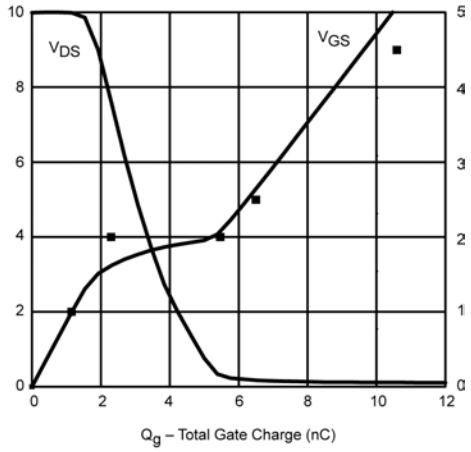






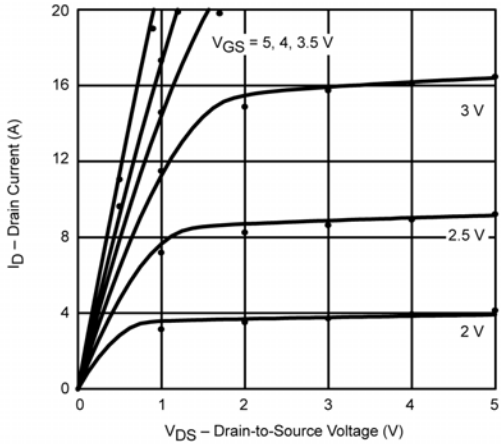


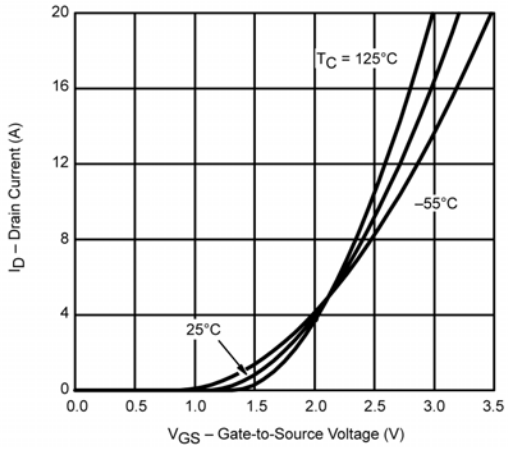


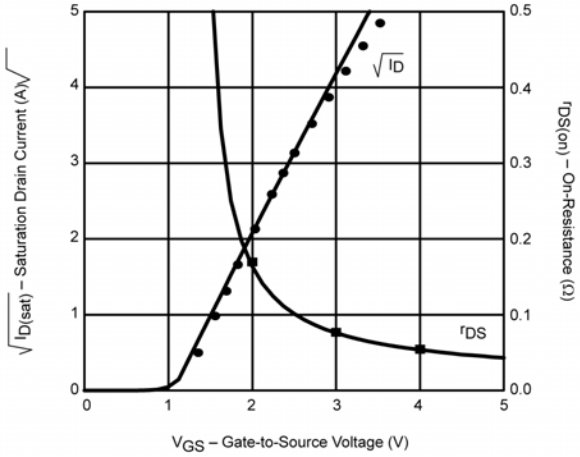


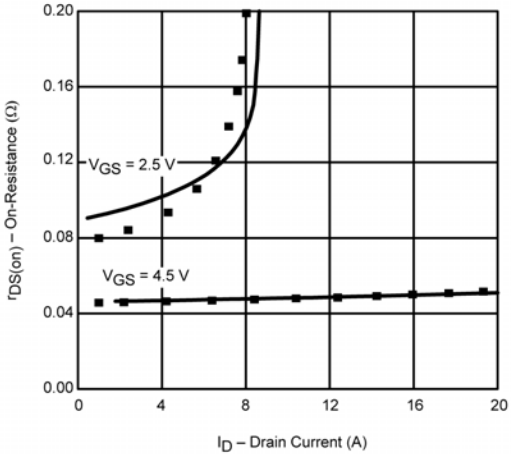
Note: Dots and squares represent measured data.

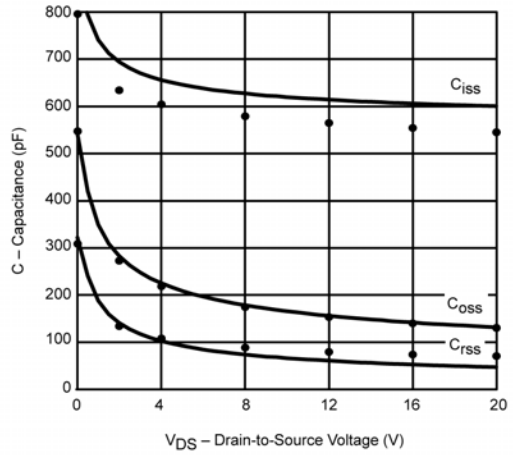
P-Channel MOSFET

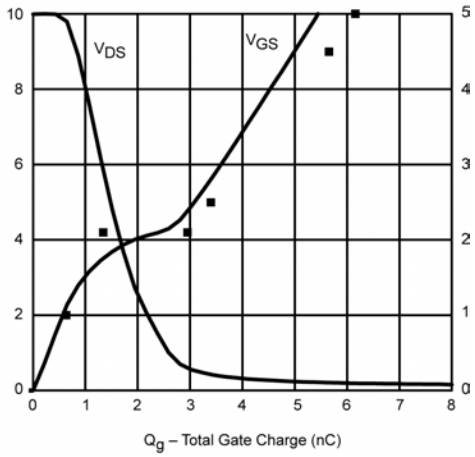












Note: Dots and squares represent measured data.

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